WHAT IS CLAIMED IS:

1. An apparatus comprising:

a sense amplifier based logic gate having an input network, said input network comprising a differential pull-down network wherein, for a stable input combination, internal nodes of said differential pull-down network are provided to one or more output nodes of said differential pull-down network.

2. The apparatus of Claim 1, wherein said differential pull down network comprises a special differential pull down network.

3. The apparatus of Claim 1, wherein said differential pull down network comprises an enhanced special differential pull down network that uses dummy transistors to form a pass-gate which is open during evaluation for a differential input.

4. The apparatus of Claim 1, wherein said differential pull down network comprises an enhanced special differential pull down network that uses dummy transistors to form a pass-gate which is always open, said pass gate inserted if different discharge paths have unequal numbers of transistors.

5. The apparatus of Claim 1, wherein during evaluation a cross-coupled inverter toggles to one state and provides a stable output when said differential pull-down network provides a path to ground.

6. The apparatus of Claim 1, further comprising a first transistor, which is always on, configured to prevent a floating node by serving as a path for sub-threshold currents.

7. The apparatus of Claim 1, further comprising differential output nodes configured to provide differential signals to a differential input.

8. The apparatus of Claim 1, wherein said differential pull-down network is configured such that each node of said differential pull-down network both a first signal and an inverse of the first signal control a transistor that loads the node.

9. The apparatus of Claim 1, further comprising a clocked transistor provided between output nodes of said logic gate such that when a clock-signal becomes low, said clocked transistor provides charge stored at one output node to partially charge said output nodes and said internal nodes to an intermediate voltage.

10. An apparatus comprising:

a sense amplifier based logic gate having an input network, said input network comprising a differential pull-up network wherein, for a stable input combination, internal nodes of said differential pull-up network are provided to one or more output nodes of said differential pull-up network.

11. The apparatus of Claim 10, wherein said differential pull up network comprises a special differential pull up network.

12. The apparatus of Claim 10, wherein said differential pull up network comprises an enhanced special differential pull up network that uses dummy transistors to form a pass-gate which is open during evaluation for a differential input.

13. The apparatus of Claim 10, wherein said differential pull up network comprises an enhanced special differential pull up network that uses dummy transistors to form a pass-gate which is always open, said pass gate inserted if different discharge paths have unequal numbers of transistors.

14. The apparatus of Claim 10, wherein during evaluation a cross-coupled inverter toggles to one state and provides a stable output when said differential pull-up network provides a path to ground.

15. The apparatus of Claim 10, further comprising a first transistor, which is always on, configured to prevent a floating node by serving as a path for sub-threshold currents.

16. The apparatus of Claim 10, further comprising differential output nodes configured to provide differential signals to a differential input.

17. The apparatus of Claim 10, wherein said differential pull-up network is configured such that each node of said differential pull-up network both a first signal and an inverse of the first signal control a transistor that loads the node.

18. The apparatus of Claim 10, further comprising a clocked transistor provided between output nodes of said logic gate such that when a clock-signal becomes low, said clocked transistor provides charge stored at one output node to partially charge said output nodes and said internal nodes to an intermediate voltage.

19. A method for transforming a differential pull-down network for a logical function, comprising:

identifying two expressions x and y that combine to the logical function according to a logical AND operation, $x.y$ corresponding to a network x and a network y;

complementing the expressions in x and y to obtain the dual expression of the logical function, as a logical OR operation, $\overline{x}+\overline{y}$;

transforming the OR operation into a transformed network $\overline{x}\cdot y+\overline{y}$, providing the transformed network to an internal node of the xy network and sharing the network y between the two branches $x\cdot y$ and $\overline{x}\cdot y+\overline{y}$; and

repeating the actions of identifying, complementing and transforming.

20. A method for transforming a differential pull-down network for a logical function, comprising:

identifying two expressions x and y that combine to the logical function according to a logical OR operation, $x + y$ corresponding to a network x and a network y;

complementing the expressions in x and y to obtain the dual expression of the logical function, as a logical AND operation, $x \cdot y$;

transforming the OR operation into a transformed network $x \cdot \overline{y} + y$, and providing the transformed network to an internal node of the $\overline{x} \cdot \overline{y}$ connection and sharing network $\overline{y}$ between the two branches $\overline{x} \cdot \overline{y}$ and $x \cdot \overline{y} + y$; and

repeating the actions of identifying, complementing and transforming.

21. A flip-flop, comprising:

an inverted input and a non-inverted input provided to an SA logic gate having first inverted and first non-inverted outputs,

said first inverted and first non-inverted outputs provided to a first set-reset latch having second inverted and second non-inverted outputs;

said inverted input, said non-inverted input, said second inverted output and said second non-inverted output provided to an SABL exclusive-or gate having inverted and non-inverted exclusive-OR outputs; and

said inverted and non-inverted exclusive-or outputs provided to a second set-reset latch having third inverted and third non-inverted outputs, said third inverted and third non-inverted outputs provided to said SABL exclusive-OR.

22. The flip-flop of Claim 12, wherein said SABL exclusive-or comprises a DPDN.

23. The flip-flop of Claim 12, wherein said SABL exclusive-or comprises a DPUN.

24. A flip-flop comprising:

a first sense-amplifier logic gate that evaluates on a falling clock edge, said

first sense-amplifier logic gate comprising a differential pull-up network, said sense-amplifier logic gate having a first inverted output and a first non-inverted output; and

said first inverted output and said first non-inverted output provided to a second sense-amplifier logic gate that evaluates on a rising clock edge, said second sense-amplifier logic gate comprising a differential pull-down network.

25. A flip-flop comprising:

a first sense-amplifier logic gate that evaluates on a rising clock edge, said first sense-amplifier logic gate comprising a differential pull-down network, said logic gate having a first inverted output and a first non-inverted output; and

said first inverted output and said first non-inverted output provided to a second sense-amplifier logic gate that evaluates on a falling clock edge, said second sense-amplifier logic gate comprising a differential pull-up network.